IN THE SPECIFICATION

Please amend the specification to read as follows:

Please insert before the first paragraph under BACKGROUND OF THE INVENTION of page 1 of the disclosure currently on file, the following paragraph:

This application is a Divisional of U.S. Serial No. 10/300,839 filed November 21, 2002, which is a Divisional of U.S. Serial No. 09/939,738 filed August 28, 2001. Priority is claimed based on U.S. Serial No. 10/300,839 filed November 21, 2002, which claims the priority of U.S. Serial No. 09/939,738 filed August 28, 2001, which claims the priority date of Japanese Patent Application No. 2000-305614 filed on October 5, 2000.

Please amend the paragraph bridging pages 12 and 13, from line 25 on page 12 through line 1 on page 13, to read as follows:

Figs. 22A - 22C are [[is a]] cross-sectional views of a principal portion of a substrate for showing a manufacturing method of a semiconductor integrated circuit device that is a fifth embodiment of the present invention.

Please amend the paragraph on page 13, from lines 2 through 5, to read as follows:

Figs. 23A - 23C are [[is a]]cross-sectional views of a principal portion of a substrate for showing the manufacturing method of a semiconductor integrated circuit device that is the fifth embodiment of the present invention.

Please amend the paragraph bridging pages 22 and 23, from line 22 on page 22 through line 3 on page 23, to read as follows:

Next, as shown in Fig. 10, a TiN film 16 is deposited on the TEOS film 13 and in each interior of the contact holes C1, C2 and C3. The TiN film 16 is patterned to thereby form intermediate wirings L1. By the intermediate wirings [[L2]] L1, the n-channel type MISFETQs and the capacitor C are connected in series. Namely, the n-type semiconductor region 7 (source and drain) of the n-channel type MISFETQs and the upper electrode 12a of the capacitor C are connected by one of the intermediate wirings L1.

Please amend the paragraph bridging pages 27 and 28, from line 19 on page 27 through line 3 on page 28, to read as follows:

Next, as shown in Fig. 18, a TEOS film S3a, a PZT film S3b used as a barrier film, and an a TEOS film S3c are sequentially deposited on the third layer wiring M3 and the interlayer insulating film S2, and thereby an interlayer insulating film S3 is formed, which consists of the above-stated films. This PZT film S3b is also an amorphous film having a Pb composition ratio of $1 + \alpha_3$ when being formed, similarly to the PZT film Slb. Next, a PIQ film [[21]] 22 is formed on the interlayer insulating film S3. The interlayer insulating film S3 and the PIQ film [[21]] 22 are formed on the uppermost layer wiring M3 and are used as films (passivation films) for protecting elements and wirings provided on the semiconductor substrate.

Please amend the paragraph on page 28, from lines 20 through 25, to read as follows:

In the present embodiment, TEOS films or the like are used to form the interlayer insulating films Sl, S2 and the like, but may also be formed by using SOG films or the like. Since a SOG film contains much moisture, forming the barrier layers Slb and S2b and the like in the interlayer insulating films Sl, S2 causes much effect.